A KYOCERA GROUP COMPANY

DC/DC Converter Output Capacitor Benchmark

R. Šponar, R. Faltus, M. Jáně, Z. Flegr, T. Zedníček

AVX Czech Republic s.r.o., Dvorakova 328, 563 01 Lanskroun, Czech Republic

email: techsales-tantalum@eur.avx.com

Abstract

Switched-mode power supplies (SMPS) are commonly found in many electronic systems. Important SMPS requirements are a stable output voltage with load current, good temperature stability, low ripple voltage and high overall efficiency. If the electronic system in question is to be portable, small size and light weight are also important considerations. A key component in switching power systems is the output capacitor – used to store the charge and for smoothing - therefore its careful selection plays a vital role in determining the overall parameters of the power supply. Different capacitor technologies – tantalum, ceramic MLCC, niobium oxide (NbO) and aluminium - are suitable to meet different electrical requirements.

This paper presents the results of an output capacitor benchmark study used in a step-down DC/DC converter design, based on a well-used control IC (Maxim's MAX 1537 – Ref.1) with a 6-24V input voltage range and two separate voltage outputs of 3.3 and 5V. The behaviour of different output capacitor technologies was evaluated by measuring the output ripple voltage. Defined fixed load and fixed switching frequency settings were used for all measurements.

Introduction

The selection of a suitable output capacitor plays an important part in the design of switching voltage converters. “Some 99 percent of so-called ‘design’ problems associated with linear and switching regulators can be traced directly to the improper use of capacitors”, states the National Semiconductor IC Power Handbook (Ref.2). The importance of the output capacitor in switching DC/DC converters is related to the fact that it is (together with the main inductor) the reservoir of electric energy flowing to the output and it smoothes the output voltage.

Today, one can hardly find a consumer, industrial or high reliability electronic device that does not make use of a voltage regulator. Designers basically use two types of regulators, linear LDO (low dropout) and step-down switch-mode DC/DC regulators to convert voltage to lower level. Switching DC/DC regulators are preferred for applications that require a greater difference between input and output voltages because they are more efficient. This switching regulator option has been selected for our experimental measurements as it is the most commonly used approach in today’s power supply circuits.

Frequency Dependence of Capacitance, ESR (effective serial resistance) and stability with operational temperature and DC bias voltage are the important parameters of output capacitors, defining performance and functionality of the complete power system. Therefore, it is these key parameters that have been measured using different capacitor technologies for the purpose of benchmarking.

Notebook computers provide one of the most demanding electronics applications where DC/DC converters are typically used with high output current requirements. Notebook supply voltages usually range between 15 and 22V with 3.3 and 5 V internal power buses commonly seen. To satisfy market demand, semiconductor manufacturers offer integrated DC/DC controllers optimized for these voltage ranges. Such controllers, soldered on a PCB together with all necessary passive and discrete components function as DC/DC converters with maximal output currents of up to several amperes. One notebook power supply converter evaluation kit, based around Maxim’s MAX1537 has been chosen as a real application example for the evaluation of different capacitor technologies.

Switched-mode power supply (SMPS) – theory and simulations

Typical SMPS topologies are shown in Figure 1. They are well documented (Ref.3).

SMPS are used for V_{IN}-to-V_{OUT} transformation:

- $V_{OUT} > V_{IN}$, realized by step-up, flyback or SEPIC converters;
- $V_{OUT} < V_{IN}$, realized by step-down, flyback or SEPIC converters;
- $V_{OUT} = V_{IN}$, realized by flyback or SEPIC converters;
- $V_{OUT} = -V_{IN}$, realized by an inverting converter.

An SMPS circuit consists of these specific parts:

- one or more switching transistors, mainly enhancement-mode MOSFETs;
- input and output smoothing capacitors;

- low-loss passive device(s) accumulating electromagnetic energy (inductors, capacitors, transformers);
- non-linear rectifying devices (plain P-N or Schottky diodes);
- control sub-circuitry for switching transistor management, feedback stability, and shut-down functionality.

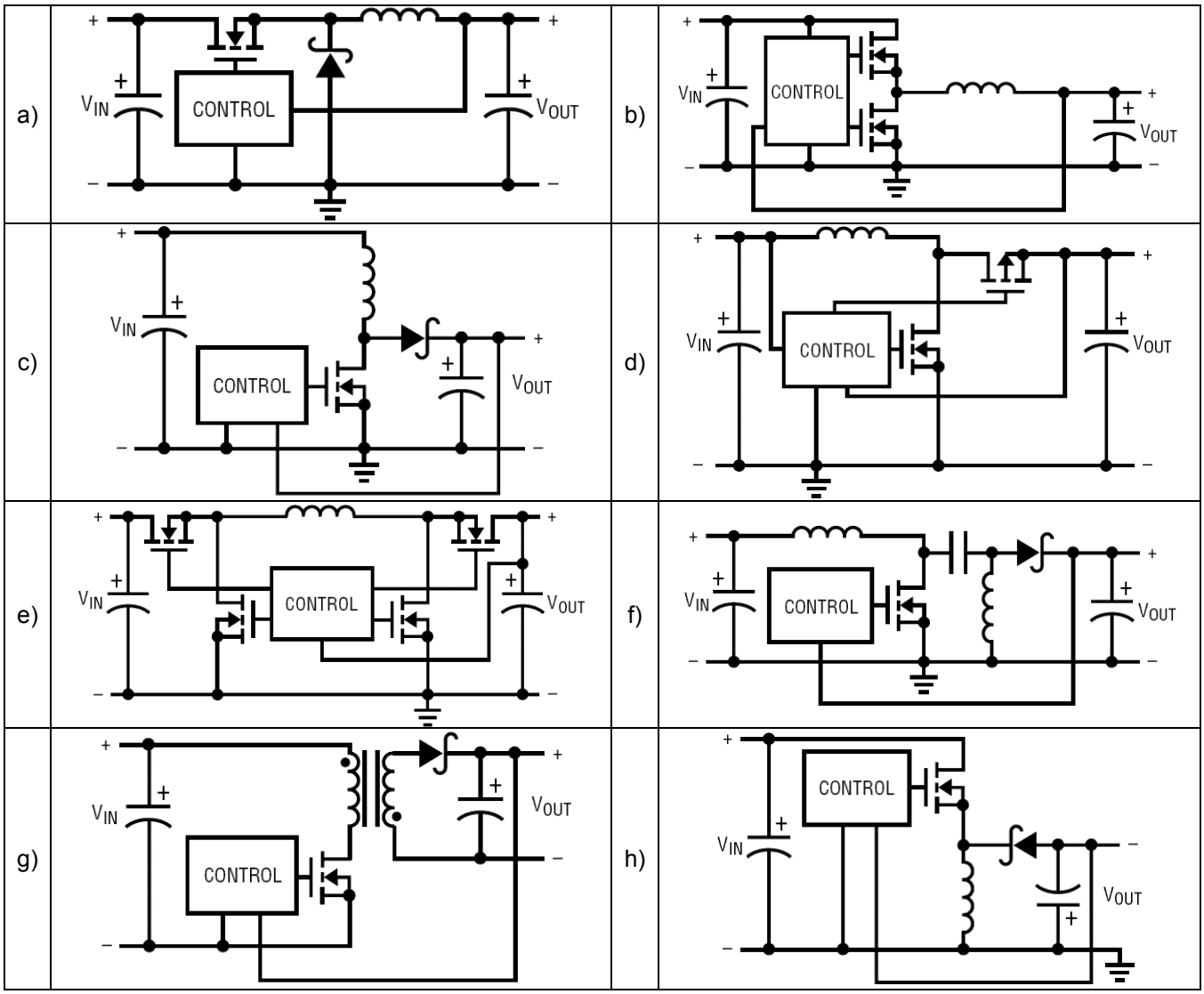


Figure 1 : Typical SMPS topologies:

a) Step-down (buck) converter
b) Synchronous step-down (buck) converter
c) Step-up (boost) converter
d) Synchronous step-up (boost) converter
e) Synchronous step-down-up (buck-boost) converter
f) Single ended primary inductor converter (SEPIC)
g) Flyback isolated-output converter
h) Inverting converter (inverter)

The SMPS function actually lies in the periodic repetition of charging and discharging cycle parts (pulse-width modulation – PWM) when the passive accumulating device(s) is (are) shortly connected to the input or output via the switching MOSFET. Switching duty cycle is the fundamental factor for V_{IN}-to-V_{OUT} transformation, i.e. determines the V_{OUT} value with respect to the V_{IN} value. Voltage drops and switching times of both rectifying diodes and switching MOSFETs are critical due to thermal parasitic losses.

Figure 2 shows a basic simulation scheme with a step-down SMPS topology based on MAX1537 Evaluation Kit

(Ref.4). OrCAD simulations express output voltage ripple dependencies on switching conditions and output capacitor properties. The circuit parameters are as follows:

$$R_{\text{input}} = 0.1\,\Omega,\ C_{\text{in}} = 10\,\mu\text{F},\ L_{\text{in}} = 3\,\text{nH},\ R_{\text{in}} = 0.1\,\Omega,\ C_{\text{inter}} = 100\,\text{nF},\ L_{\text{ser}} = 6\,\mu\text{H},$$
$$C_{\text{out}} = 1\,\text{mF}\,(\text{basic value}),\ L_{\text{out}} = 3\,\text{nH},\ R_{\text{out}} = ESR = 10\,\text{m}\Omega\,(\text{basic value}),\ R_{\text{load}} = 1\,\Omega,$$
$$\text{MOS Switch: } R_{\text{on}} = 25\,\text{m}\Omega,\ R_{\text{off}} = 1\,\text{M}\Omega,\ t_{\text{switch}} = 2.5\,\text{ns},\ t_{\text{delay}} = 35\,\text{ns}.$$

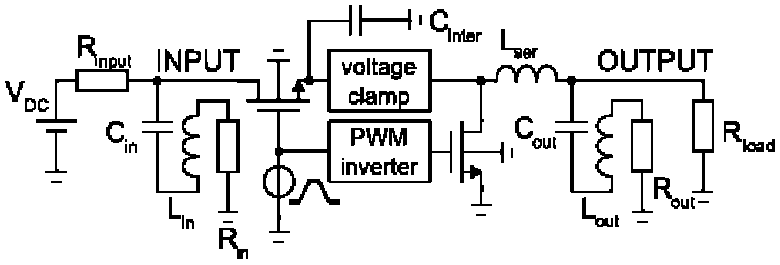


Figure 2 : SMPS simulation scheme

Figure 3 shows that the output voltage ripple depends on the switching frequency and the duty cycle factor. V_{DC} was set at 7V. Obviously the optimal switching frequency lies between 100 kHz and 1MHz while the duty cycle factor linearly affects the DC output voltage.

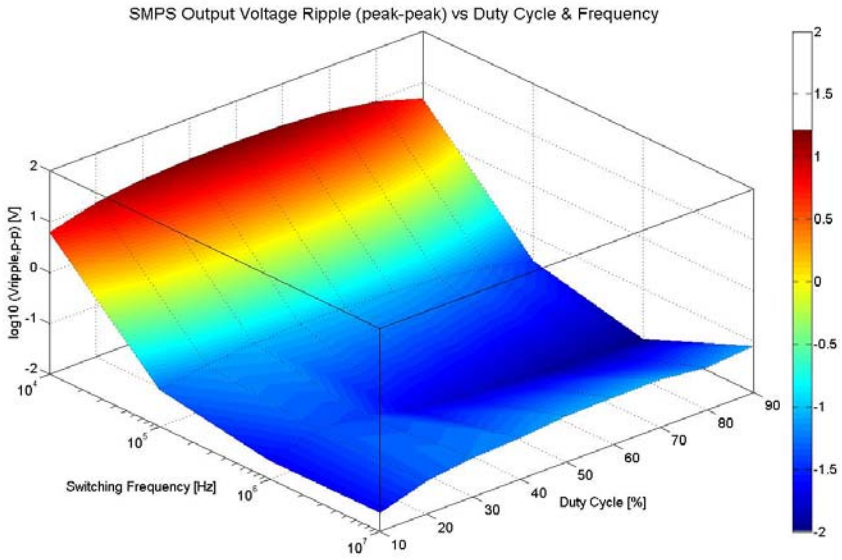


Figure 3 : SMPS output voltage ripple (dependent on frequency and duty cycle)

Figure 4 shows the output voltage ripple dependency on output capacitor ESR and capacitance. V_{DC} was set at 20V, switching frequency is 300 kHz and the duty cycle is 17%. The lowest ripple values can be obtained when 100μF < C < 1mF and ESR < 0.1Ω are used.

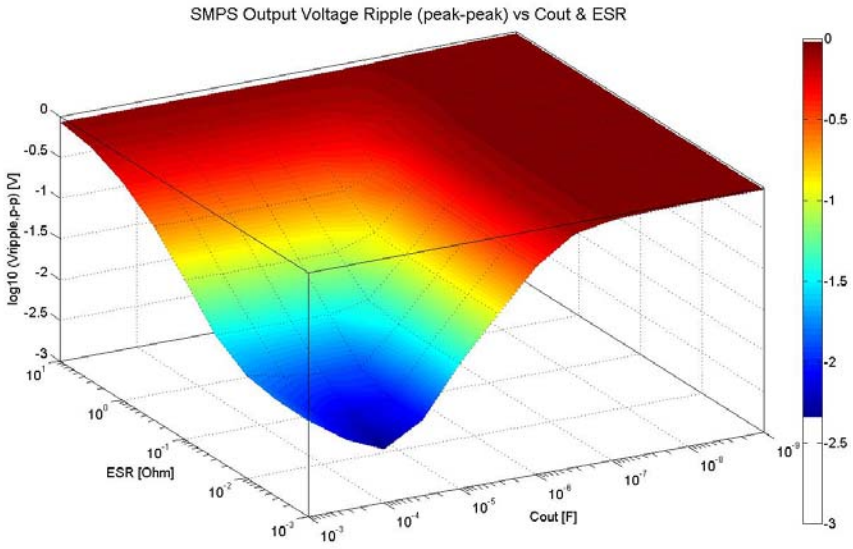


Figure 4 : SMPS output voltage ripple (dependent on output capacitor ESR and C)

Low Drop-Out Regulator (LDO) - theory and simulations

There are two functions of a capacitor connected to the output of an LDO:

- Local electrical energy reserve
- RF noise coupling to ground
- Feedback stability factor for LDO

A simplified structure of an LDO with external input/output capacitor and feedback resistors is shown in Figure 5.

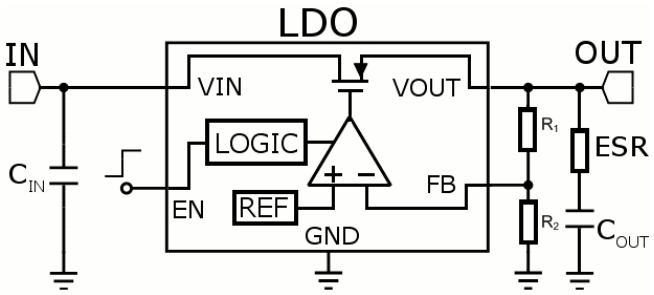


Figure 5 : Simplified LDO and typical external components

It is commonly known that the output capacitor influences the stability of an LDO with a connected load (assumed to be pure resistive). Note that the type of switching transistor used in the LDO structure corresponds to the orientation of positive /negative inputs of an amplifier within the LDO feedback loop. The following transistors can be utilized: NPN or PNP in case of BJT; and N-channel or P-channel in case of enhancement and depletion mode MOS. NPN and N-channel MOS transistors are implemented as shown in Figure 5; PNP and P-channel MOS require the amplifier inputs to be swapped. The feedback is designed to lead the voltage signal from the voltage $R_2/(R_2+R_1)$ divider to the signal-error voltage amplifier (both VFA and CFA), which is DC

biased on one input and asymmetrically supplied (V_{IN} to GND).

We are able to describe LDO properties that may influence the LDO feedback stability:

- input impedance of the feedback amplifier (much greater than both the external feedback resistors R_1, R_2);
- parasitic grounded impedance of connected open output mirror and voltage follower;
- input impedance of the feedback amplifier (much lower than the input impedance of the switching transistor);
- switching transistor parameters, mainly gate-source, gate-drain and drain-source capacitance;
- frequency characteristics of the over-current feedback loop.

Major aspects playing an important role in LDO feedback stability will be analysed:

- two-pole amplifier (single-pole, unity-gain voltage followers, single-pole, open output current mirror);
- Giacoletto model of switching MOS transistor (based on voltage-controlled current source)

The LDO stability is often evaluated from the open loop scheme shown in Figure 6.

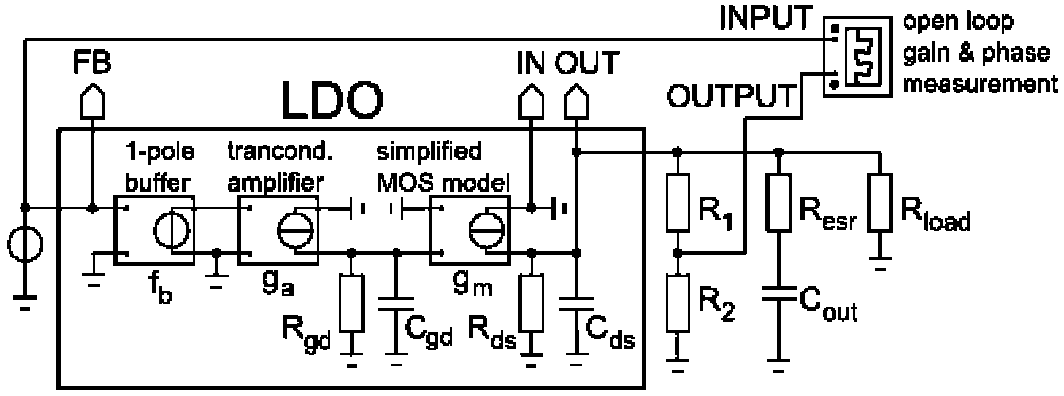


Figure 6 : Open loop gain & phase measurement of LDO with external resistive divider, output capacitor and load

The voltage open loop transfer function can be stated as follows:

$$\boldsymbol{K}_{\mathrm{V}} = \frac{2\pi f_{\mathrm{b}}}{\boldsymbol{s}+2\pi f_{\mathrm{b}}} \cdot \frac{g_{\mathrm{a}}}{C_{\mathrm{gd}}} \cdot \frac{1}{\boldsymbol{s}+\dfrac{1}{C_{\mathrm{gd}}R_{\mathrm{gd}}}} \cdot \frac{g_{\mathrm{m}}}{C_{\mathrm{ds}}} \cdot \frac{\boldsymbol{s}+\dfrac{1}{C_{\mathrm{out}}R_{\mathrm{esr}}}}{\left(\boldsymbol{s}+\dfrac{1}{C_{\mathrm{out}}R_{\mathrm{esr}}}\right)\left(\boldsymbol{s}+\dfrac{R_{\mathrm{ds}}^{-1}+R_{\mathrm{load}}^{-1}+\left(R_1+R_2\right)^{-1}}{C_{\mathrm{ds}}}\right)+\dfrac{\boldsymbol{s}}{C_{\mathrm{ds}}R_{\mathrm{esr}}}} \cdot \frac{R_2}{R_1+R_2},$$

where f_B is a dominant pole frequency of the feedback voltage buffer, g_a is a gain of the feedback transconductance amplifier, and g_m is the transconductance gain of the Giacoletto model of the switching MOS transistor. The 'gd' and 'ds' index refers to the MOS gate-drain and drain-source resistance/capacitance respectively. R_{esr} and C_{out} represent the elementary model of the output capacitor and R_{load} means the resistive

load.

If a designer adds a capacitor to the LDO output, the voltage open loop transfer function changes with the ratio:

$$\boldsymbol{R} = \frac{\boldsymbol{K}_{\mathrm{V,with\_capacitor}}}{\boldsymbol{K}_{\mathrm{V,without\_capacitor}}} = 1 - \frac{\dfrac{\boldsymbol{s}}{C_{\mathrm{ds}}R_{\mathrm{esr}}}}{\dfrac{\boldsymbol{s}}{C_{\mathrm{ds}}R_{\mathrm{esr}}} + \left(\boldsymbol{s} + \dfrac{R_{\mathrm{ds}}^{-1} + R_{\mathrm{load}}^{-1} + \left(R_1 + R_2\right)^{-1}}{C_{\mathrm{ds}}}\right)\left(\boldsymbol{s} + \dfrac{1}{C_{\mathrm{out}}R_{\mathrm{esr}}}\right)}.$$

The reader can confirm that in the case $R_{\mathrm{esr}} \to \infty\ \Omega$ or $C_{\mathrm{out}} \to 0$ F the $\boldsymbol{R} \to 1$.

$\boldsymbol{K}_{\mathrm{V}}$ function of LDO without the output capacitor contains plain real poles with characteristic frequencies:

$$f_{\mathrm{p1}} = f_{\mathrm{b}},\ f_{\mathrm{p2}} = \frac{1}{2\pi C_{\mathrm{gd}}R_{\mathrm{gd}}},\ f_{\mathrm{p3}} = \frac{R_{\mathrm{ds}}^{-1} + R_{\mathrm{load}}^{-1} + \left(R_1 + R_2\right)^{-1}}{2\pi C_{\mathrm{ds}}}\ \left[\mathrm{Hz}\right]$$

Adding the output capacitor we obtain the plain real zero (f_{z1}) and the pseudo-pole (f_{p4}) due to $\boldsymbol{s}/C_{\mathrm{ds}}R_{\mathrm{esr}}$ element:

$$f_{\mathrm{z1}} = \frac{1}{2\pi C_{\mathrm{out}}R_{\mathrm{esr}}},\ f_{\mathrm{p4}} \approx \frac{1}{2\pi C_{\mathrm{out}}R_{\mathrm{esr}}}\ \left[\mathrm{Hz}\right]$$

Due to the pseudo-pole existence, the single zero is not eliminated by the pseudo-pole and has an ability to increase the LDO stability.

The well-known Bode criterion states that a feedback electrical system is stable if the open loop magnitude curve crosses unity-gain level with a maximum slope of less than 30 dB/decade. Absolute stability is obtained when the slope is lower or equal to 20 dB/decade, therefore the unity gain phase margin is positive.

Let us assume following numerical values of the scheme shown in Figure 6:

$$f_{\mathrm{b}} = 10\ \mathrm{kHz},\ g_{\mathrm{a}} = g_{\mathrm{m}} = 100\ \mathrm{mS},\ C_{\mathrm{gd}} = 100\ \mathrm{pF},\ R_{\mathrm{gd}} = 10\ \mathrm{M\Omega},\ C_{\mathrm{ds}} = 1\ \mathrm{nF},\ R_{\mathrm{ds}} = R_{\mathrm{load}} = 10\ \Omega,$$
$$R_1 = 10\ \mathrm{k\Omega},\ R_2 = 1\ \mathrm{k\Omega},\ C_{\mathrm{out}} \in \langle 10\ \mathrm{nF};\ 1\ \mathrm{mF}\rangle,\ R_{\mathrm{esr}} \in \langle 1\ \mathrm{m\Omega};\ 100\ \Omega\rangle.$$

If the typical value of DC reference voltage is V_{ref} = 1.25 V, then the output DC voltage and output load current is:

$$V_{\mathrm{out}} = V_{\mathrm{ref}} \cdot \frac{R_1 + R_2}{R_2} = 13.75\ \mathrm{V},\ I_{\mathrm{out}} = \frac{V_{\mathrm{out}}}{R_{\mathrm{load}}} = 1.375\ \mathrm{A}.$$

The numerical values of pole characteristic frequencies of LDO without the output capacitor are as follows:

$$f_{\mathrm{p1}} = 10\ \mathrm{kHz},\ f_{\mathrm{p2}} = 159\ \mathrm{Hz},\ f_{\mathrm{p3}} = 31.8\ \mathrm{MHz}.$$

An LDO application designer should know the capacitance and ESR of the output capacitor. Figure 7 shows how the unity gain frequency (transient frequency) changes with varying C_{out} and R_{esr}. It appears that by using as high capacitance and as low ESR as possible leads to the lowest transient frequency.

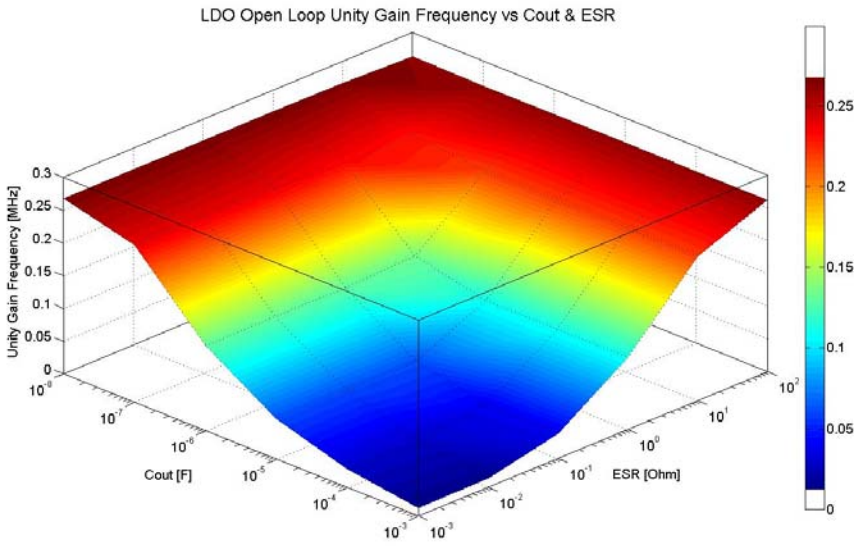


Figure 7 : Capacitance and ESR of output capacitor influence unity gain frequency of LDO regulation loop

Figure 8 displays an example of LDO open loop phase margin at 1 MHz and proves the phase margin insensitivity to ESR changes, especially for C_{out} > 100 μF. The transient frequency point may be lower or greater than 1 MHz (dependent certainly on C_{out} and *ESR*). As a worst case scenario, we need the positive phase margin for the band up to the transient frequency. Figure 8 proves that a too low ESR solution leads to undesired negative phase margin at lower C_{out}.

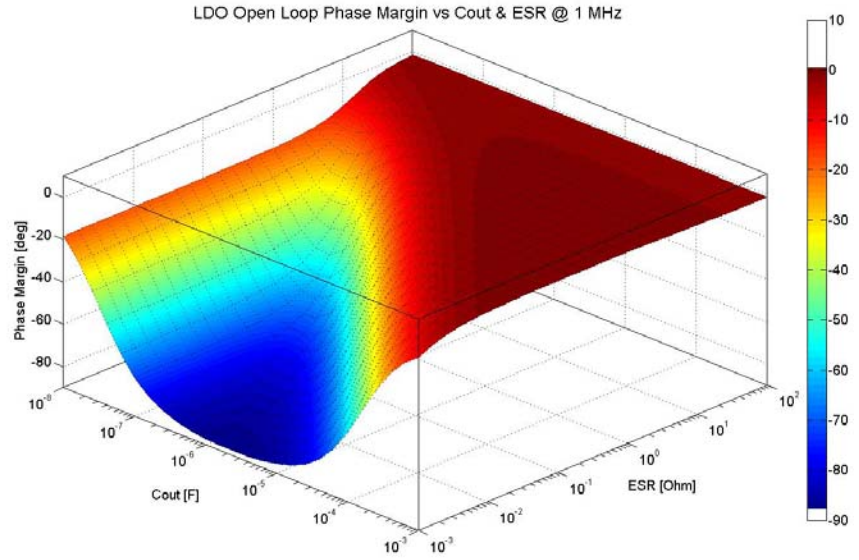


Figure 8 : LDO regulation loop phase margin @ 1 MHz

Figure 9 shows the real worst case phase margin and was obtained using iterative computations over the transient frequency space. The phase margin is always positive if $C_{\text{out}} > 100\ \mu\text{F}, R_{\text{esr}} \approx 0.1\ \Omega$. This conclusion is certainly valid only for the given numerical values of internal LDO parameters as well as external properties (i.e. resistive feedback voltage divider and output load). Both C_{out} and R_{esr} fundamentally change a zero point position and thus shift the phase margin value in the positive-gain band.

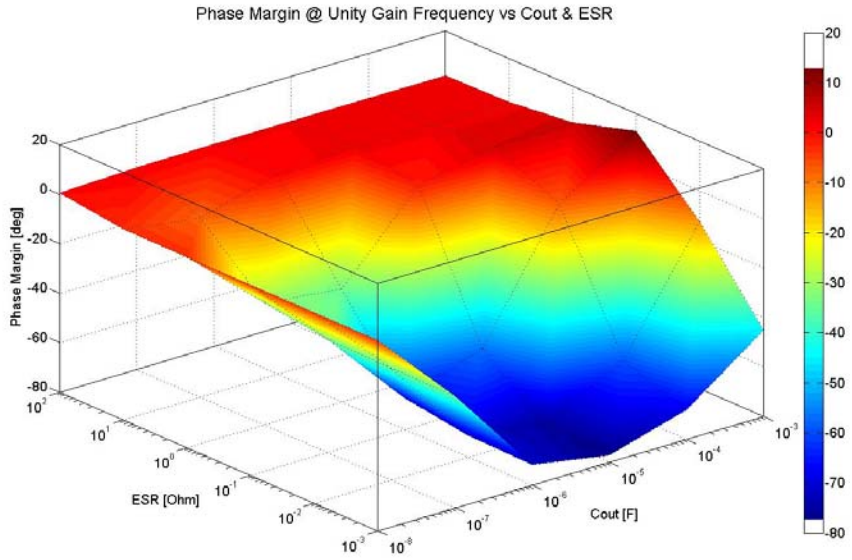


Figure 9 : Worst case: LDO open loop phase margin @ unity gain frequency

Previous symbolic and numerical computations as well as 3D graphs gave the answer to the question: "How will a capacitor affect the LDO stability." It is clear that an LDO application designer should search for a valid LDO model and verify the LDO stability in two ways:

- Open loop AC stability analysis (gain & phase margin evaluation);
- Steep input edge transient analysis of the output signal stability and settling (power-on testing).

A numerical circuit simulation with precise LDO/SMPS and output capacitor models gives more credible results in a shorter time than elaborating rigorous semi-symbolic computations as shown above. The previous mathematical apparatus only wants to show the possibility to guess the right C_{out} and *ESR* values.

Measurement set-up

Initially, the frequency characteristics of capacitance and ESR of two capacitor groups was measured. The first group included different capacitors specified for the 3.3V output with capacitance C = 220µF; the second group contained capacitors for the 5V output where C = 150µF. Electrical parameters were measured using an HP 4194A impedance/gain-phase analyser (Ref. 5) in a frequency range of 120Hz to 1MHz (capacitance) and 120Hz to 10MHz (ESR).

The temperature stability of the converter is one of industry's most common requirements. Thus, the second measurement concentrated on capacitance and ESR stability with temperature and DC voltage bias. The 3.3V output capacitor group was measured using an HP 4192A impedance analyser and a Keithley 7002 switch

system across the DC bias, voltage range 0 – 4V, conditioned in a Votsch VC 7018 laboratory oven over the temperature range of -55 to +125degC.

Maxim Integrated Product's MAX1537EV KIT (Ref. 4) converter was used for the benchmarking tests. The evaluation kit provides two power outputs, 3.3 and 5 V, both with a maximum current I_{out} of 5A. A photograph of the kit is shown in Figure 10. The recommended output capacitance, C, for the 3.3V output is 220µF (see position C6 in Figure 11); for the 5V output the value of C is 150µF. AC ripple voltage values and wave forms were used as the main indicator of filtering quality. A Goldstar GP-505 stabilized power supply was used to supply the kit with a fixed input voltage V_{in} of 20V.

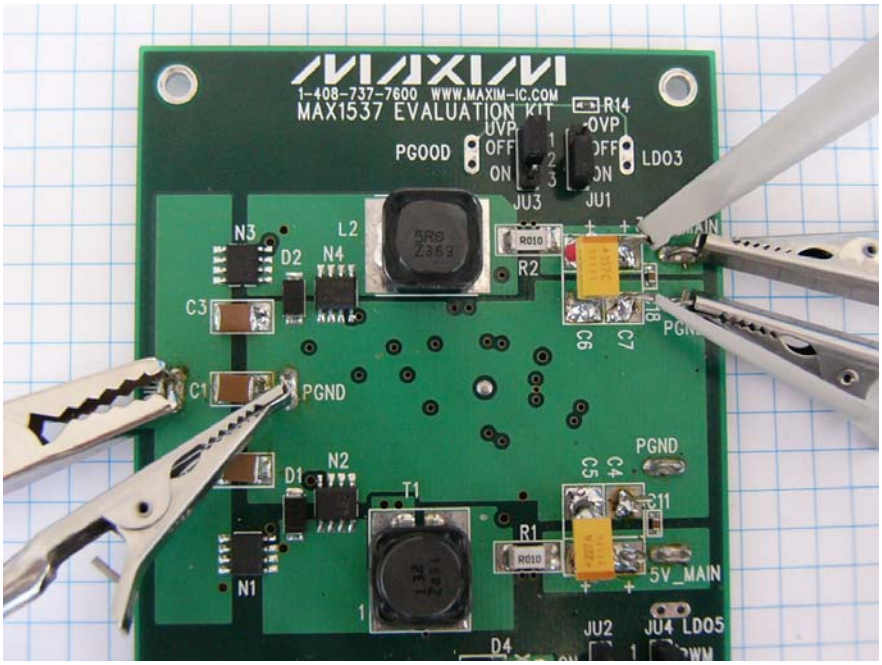


Figure 10 : MAX1537EV evaluation kit

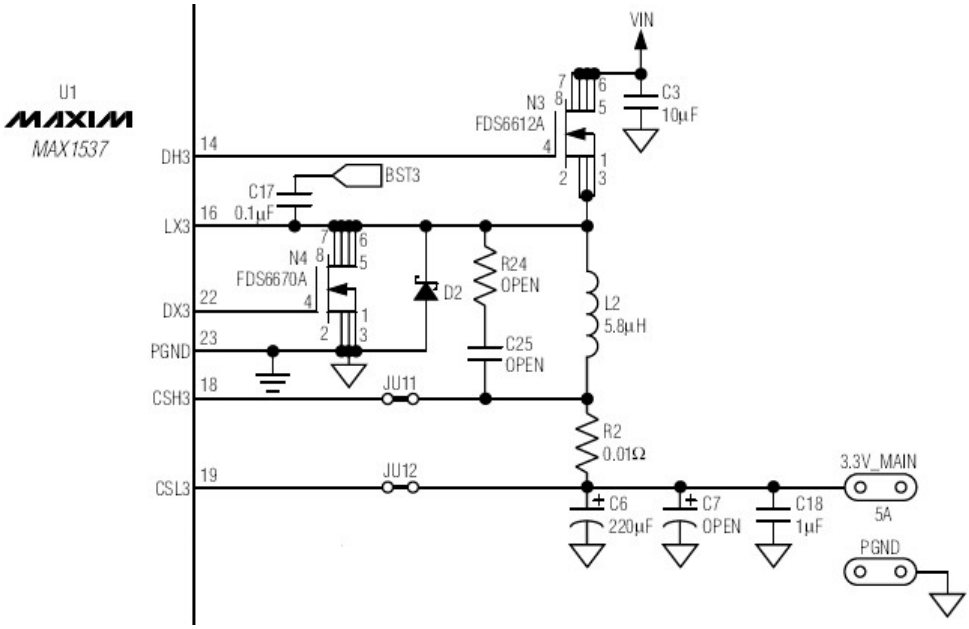


Figure 11 : Section of the MAX1537EV evaluation kit schematic diagram with 3.3V output

An output load was set up using resistors and capacitors to draw two thirds of the maximum current. (For 3.3V output this was a parallel combination of 2.2 Ω resistor (R) and 4.7µF tantalum capacitor (C); for the 5V output the value of R=3.2Ω (see Figure 12). Voltage waveforms and relevant AC Vrms (effective value) were displayed using an Agilent Infiniium 54830B digital oscilloscope (Ref. 6).

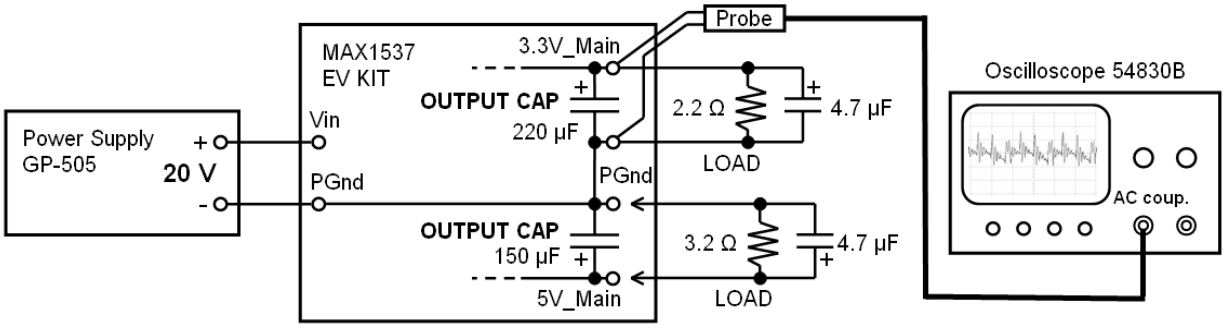


Figure 12 : MAX1537EV evaluation kit measurement connection diagram

Frequency characteristics of various capacitors used for 3.3 V output

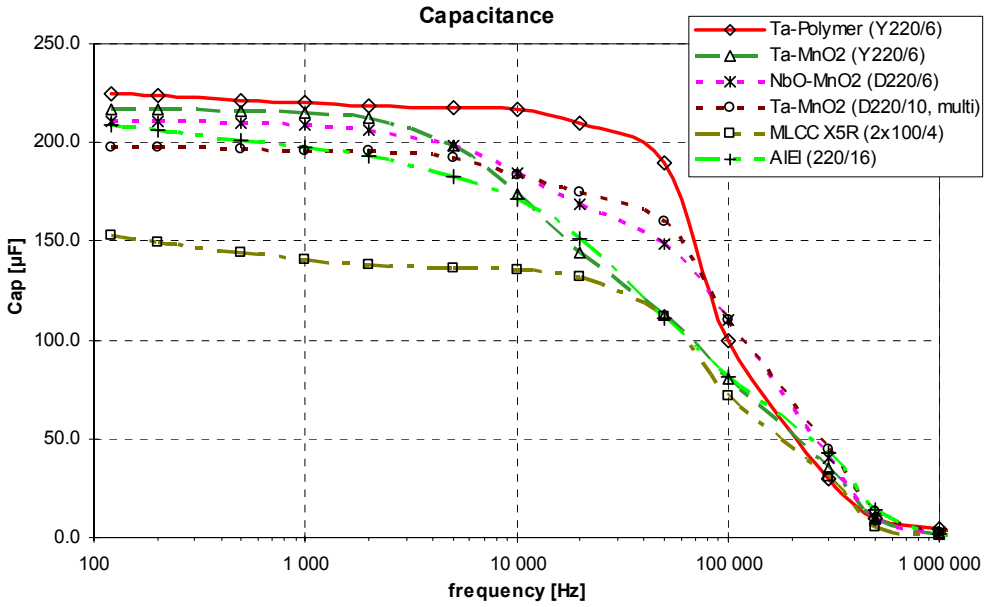


Figure 13 : Capacitance vs. frequency of various capacitors for 3.3V output

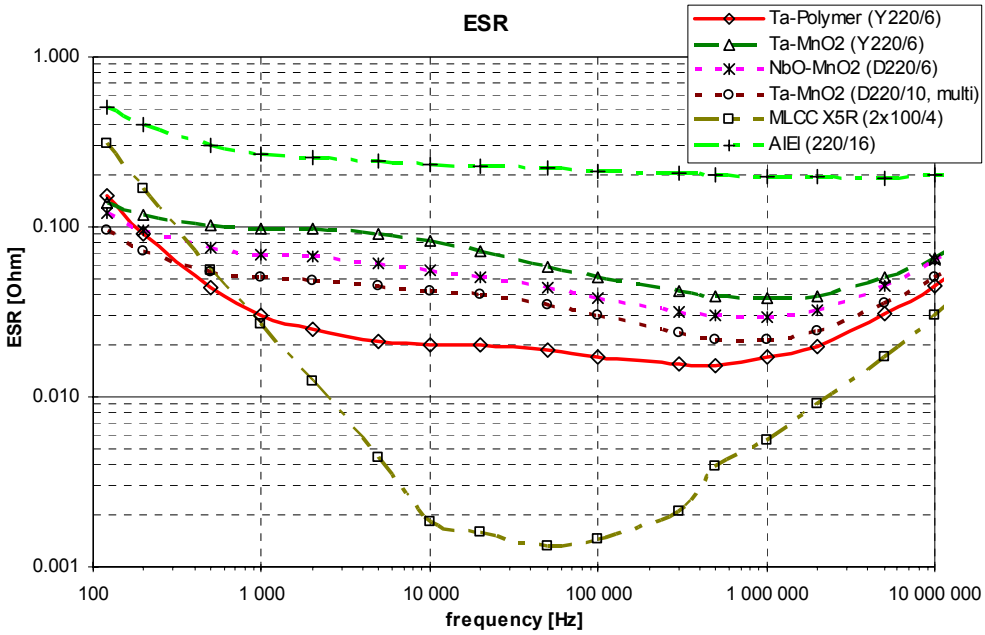


Figure 14 : ESR vs. frequency of various capacitors for 3.3V output

The graphs above show the frequency characteristics of several different technology capacitors used for the 3.3V evaluation kit output with nominal capacitance C = 220µF (except MLCC where two parallel 100µF were used). The capacitor technologies chosen were Tantalum-Polymer, Tantalum-MnO_2 (single and multi-anode construction), Niobium Oxide-MnO2, Multilayer Ceramic, and Aluminium Electrolytic.

We can observe a relatively small drop in capacitance in the frequency range 10 – 100kHz in the case of Tantalum-Polymer and Tantalum-MnO_2 multi-anode construction capacitors (see Figure 15), whereas Tantalum-MnO_2 and Aluminium-electrolytic capacitors exhibit a larger drop across the same range. The actual capacitance of the MLCC capacitor suffers due to its dependence on the DC bias voltage, which was applied during measurement. The very low ESR performance of the MLCC parts, and still relatively low ESR of the Tantalum-Polymer capacitors is shown in Figure 16. The ESR of Aluminium-electrolytic capacitors is relatively high over the complete measured frequency range.

Frequency characteristics of various capacitors chosen for 5V output

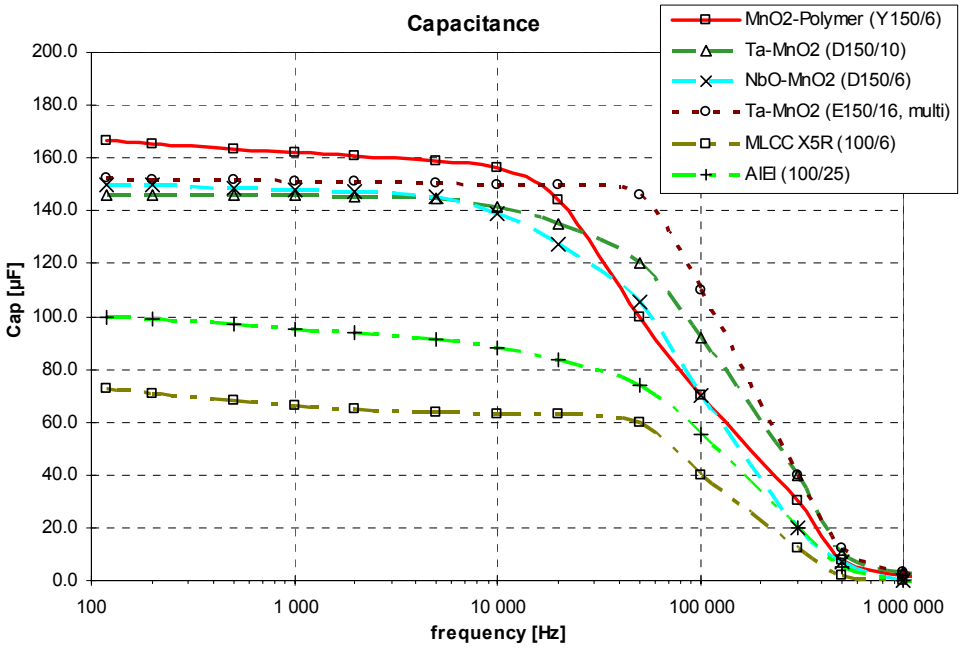


Figure 15 : Capacitance vs. frequency of various capacitors for 5V output

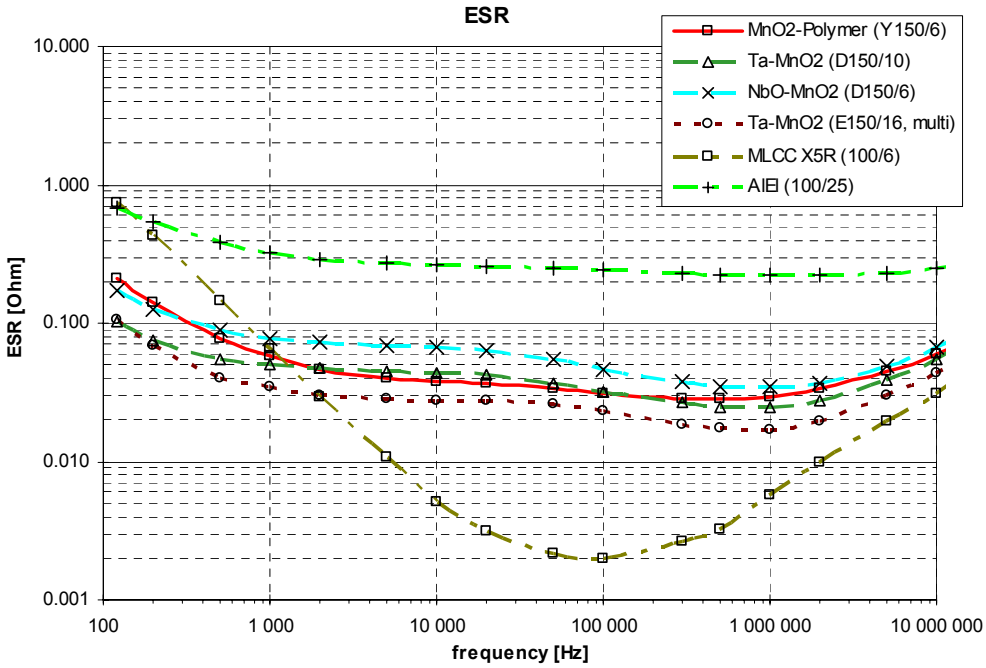


Figure 16 : ESR vs. frequency of various capacitors for 5V output

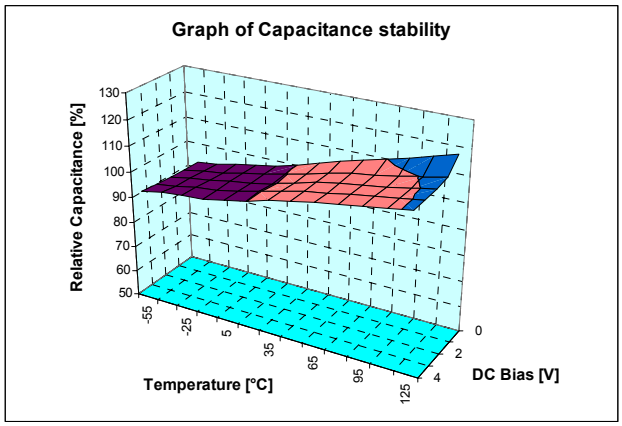
The graphs above show the frequency characteristics of different technology capacitors used with the 5V evaluation kit output with nominal capacitance (C) of 150µF (except MLCC (100µF) and AlEl (100µF)). (Technologies as for the 3.3V output tests, detailed in the paragraph above.)

Both Tantalum-MnO_2 single and multi-anode capacitors retain a higher capacitance at higher frequencies (above 100kHz), whereas Niobium Oxide-MnO_2 and Aluminium electrolytic capacitors lose their capacitance faster at lower frequencies (see Figure 15). MLCC exhibits very low ESR around the 100kHz frequency range; Tantalum-MnO_2 multi-anode and Tantalum-Polymer capacitors show low ESR in the same

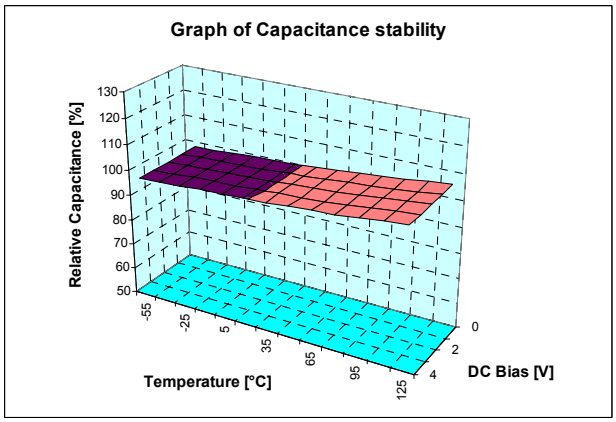
frequency range, whereas Aluminium electrolytic devices have a high ESR over all frequency ranges.

Capacitance stability vs. DC bias voltage and temperature

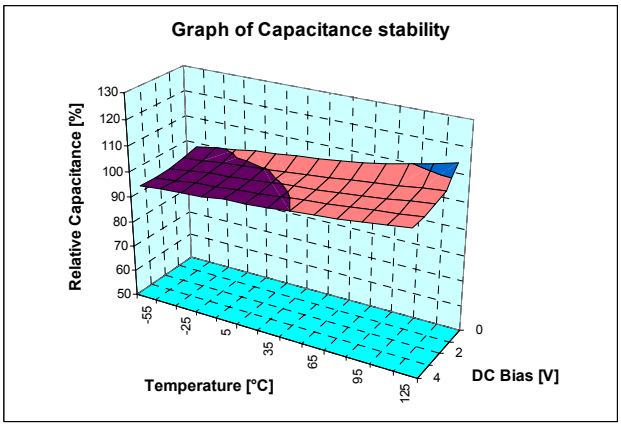
Ta-Polymer (case Y 220µF / 6V)



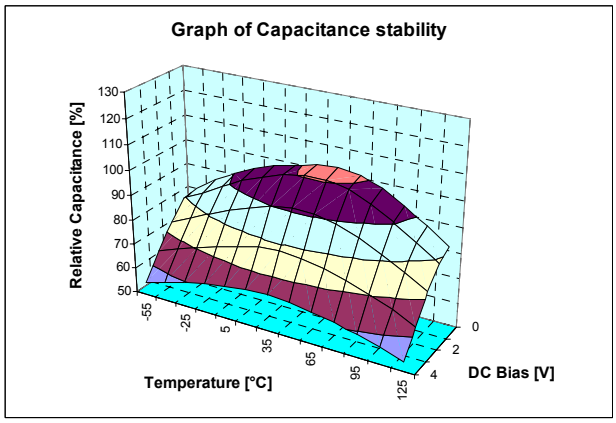
Ta-MnO_2 (case Y 220µF / 6V)



NbO-MnO_2 (case D 220µF / 6V)



MLCC X5R (2 x 100µF / 4V)



AlEl (220µF / 16V)

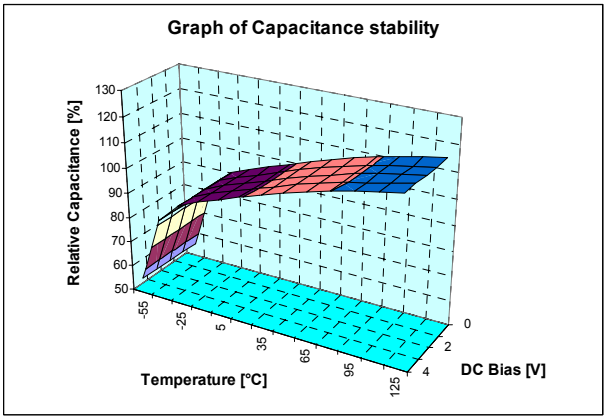


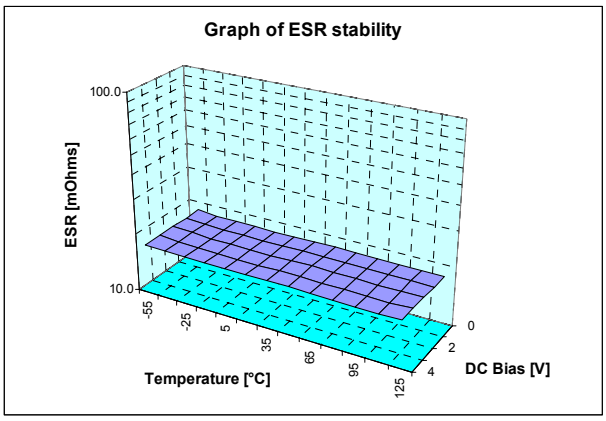
Figure 17 : Capacitance stability of various capacitors for the 3.3V evaluation kit output

The experiments showed that the best overall capacitance stability is exhibited by Tantalum-MnO2 technology

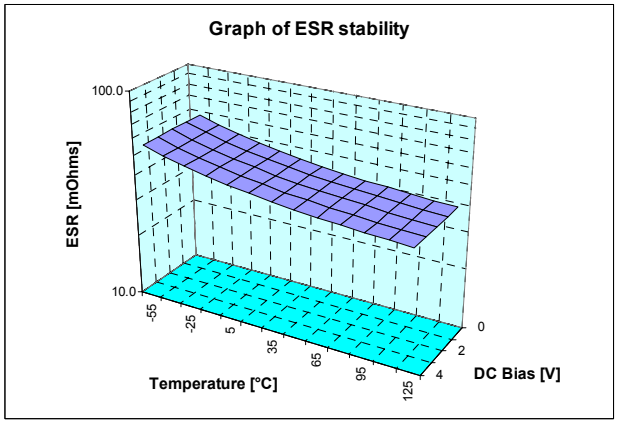
capacitors (see Figure 17). The capacitance of Niobium Oxide-MnO2 devices is more sensitive to DC bias voltage, while Tantalum-Polymer is more sensitive to temperature changes. The capacitance of MLCC devices is very dependent on both actual temperature and DC bias. The capacitance of Aluminium electrolytic capacitors is stable with DC bias but very dependent on temperature.

ESR stability vs. DC bias voltage and temperature

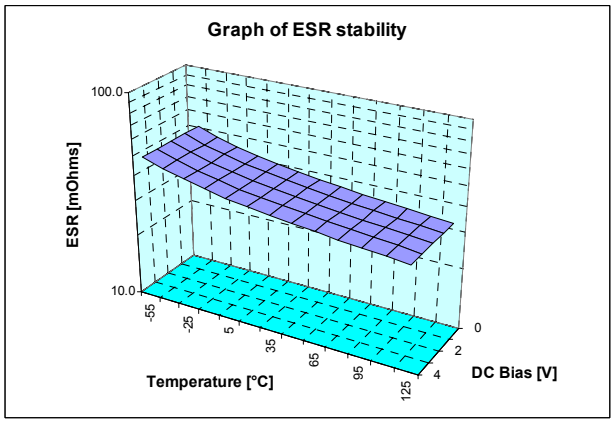
Ta-Polymer (case Y 220µF / 6V)



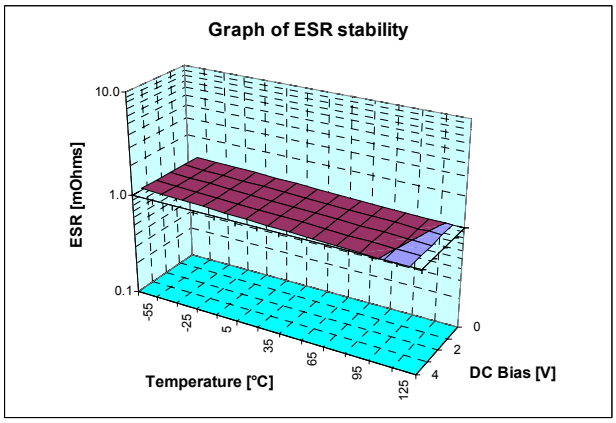
Ta-MnO_2 (case Y 220µF / 6V)



NbO-MnO_2 (case D 220µF / 6V)



MLCC X5R (2 x 100µF / 4V)



AlEl (220µF / 16V)

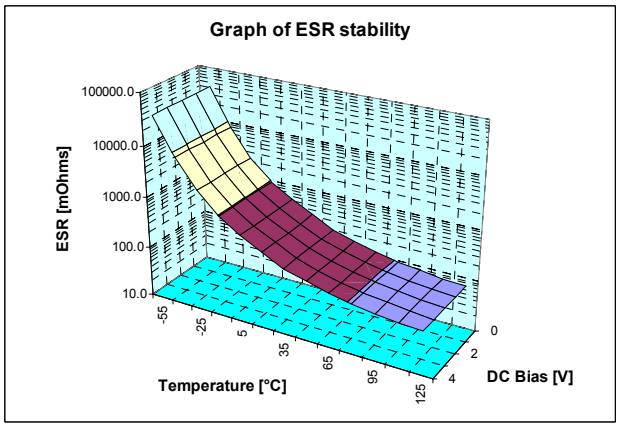
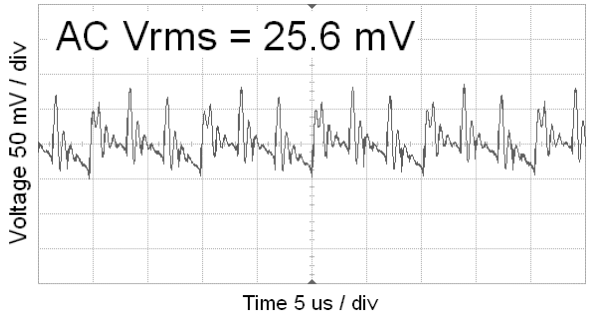


Figure 18 : ESR stability of various capacitors dedicated for 3.3 V evaluation kit output

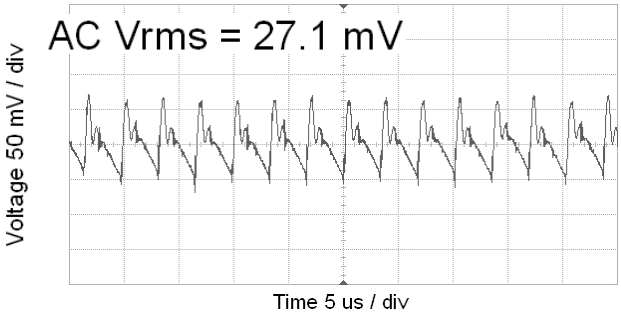
We can see that ESR is relatively stable vs. DC bias voltage for all capacitors. However, differences can be seen when we compare ESR stability versus temperature (see Figure 18). Tantalum-Polymer and MLCC capacitors exhibit the most stable ESR, and the ESR of MLCC devices is very low over the whole temperature range. With Tantalum-MnO_2 and Niobium Oxide-MnO_2 components, ESR decreases as temperature increases. Aluminium electrolytic capacitors behave differently: ESR grows to very high values at low temperatures (below 0degC), due to the limitation of wet electrolyte conductivity at low temperatures.

DC/DC converter output ripple voltage waveform

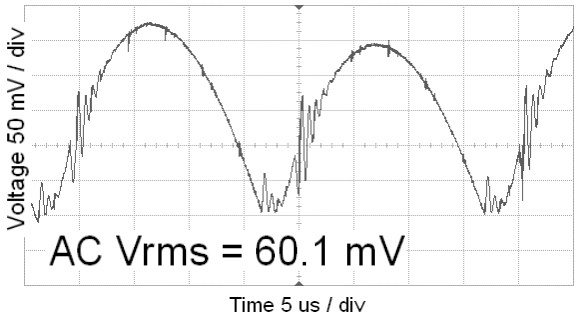
3.3 V line – Ta-Polymer (case Y 220µF / 6V)



3.3 V line – Ta-MnO_2 (case Y 220µF / 6V)



3.3 V line – MLCC X5R (2 x 100µF / 4V)



3.3 V line – AlEl (220µF / 16V)

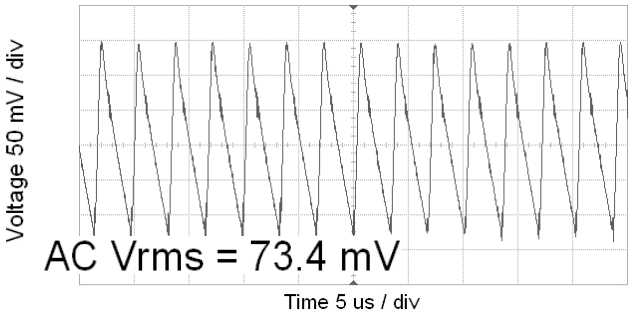
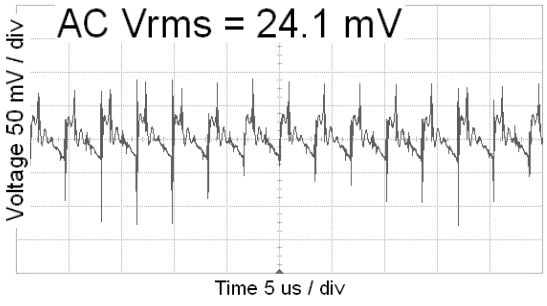
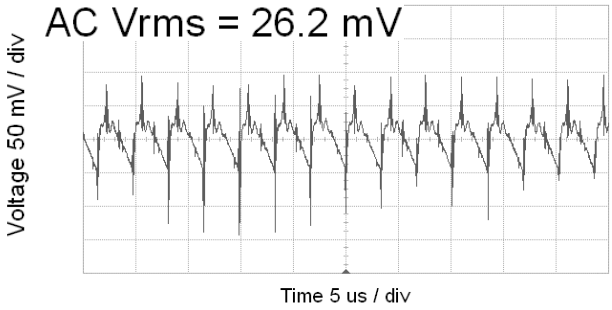


Figure 19 : Output ripple current waveforms on the 3.3V rail with selected capacitors

5 V line – Ta-Polymer (case Y 150µF / 6V)



5 V line – NbO-MnO_2 (case D 150µF / 6V)



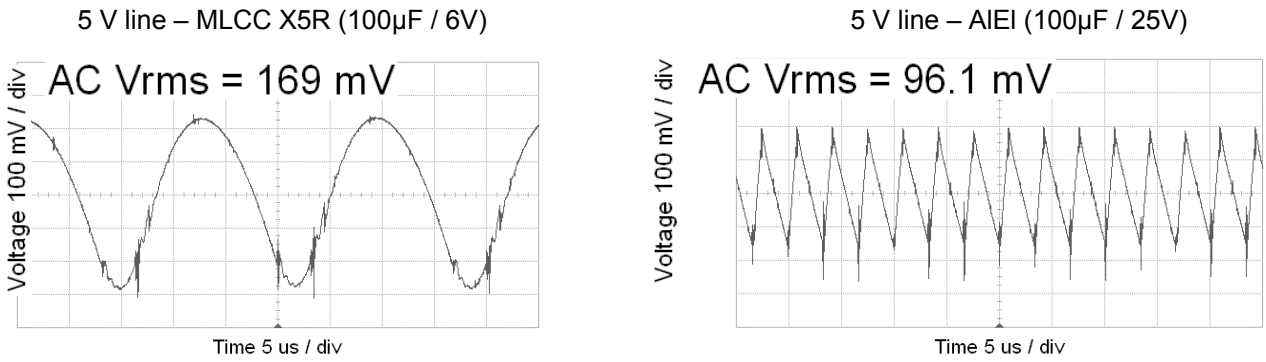


Figure 20 : Output ripple current waveforms on the 5V rail with selected capacitors

Figure 19 and Figure 20 show the different waveform shapes that occur when different capacitors types are used. Comparing Tantalum-Polymer and Tantalum-MnO_2 capacitors shows that the ripple voltage using Tantalum-MnO_2 devices contains a lower level of higher harmonic components for both 3.3 and 5V outputs. The basic frequency of the ripple voltage is naturally equal to the switching frequency of the converter (f_{sw} = 300 kHz). When using MLCC capacitors, both 3.3 and 5V circuits exhibited undesirable oscillations (f_{osc} approximately = 50 kHz) and high AC Vrms due to the regulator instability. Aluminium electrolytic types did not perform well, as can be seen on the waveforms of both outputs measured by a relatively high AC Vrms.

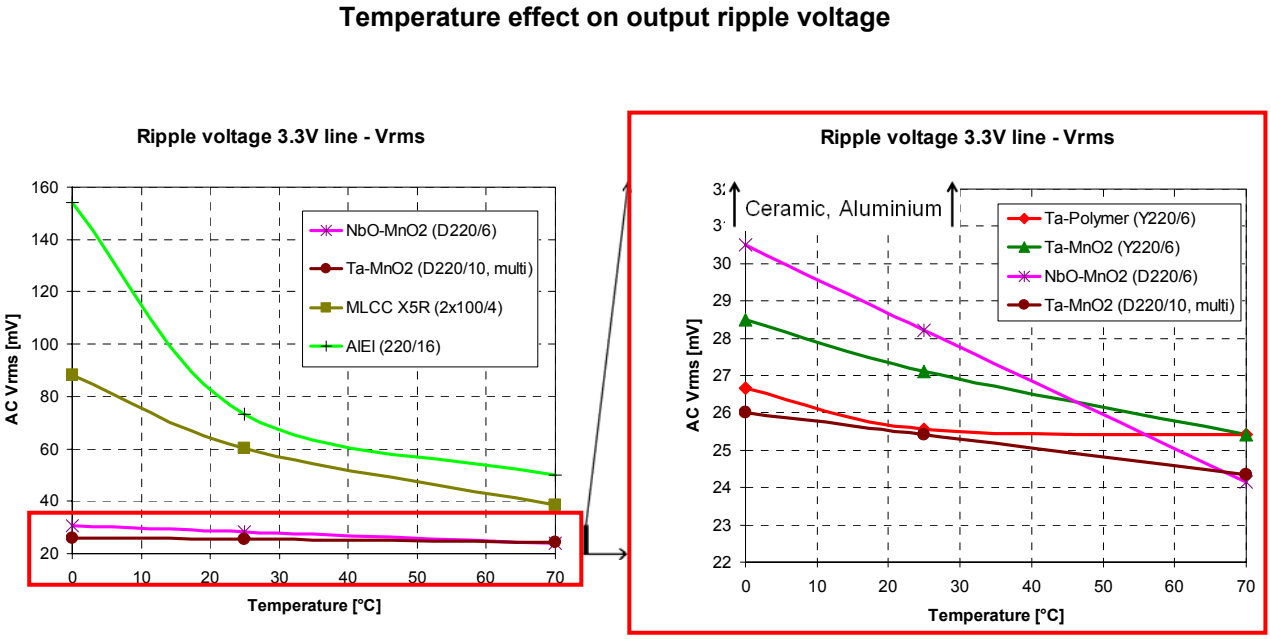


Figure 21 a: b:

3.3V output Vrms of ripple voltage benchmark, magnified scale on right side

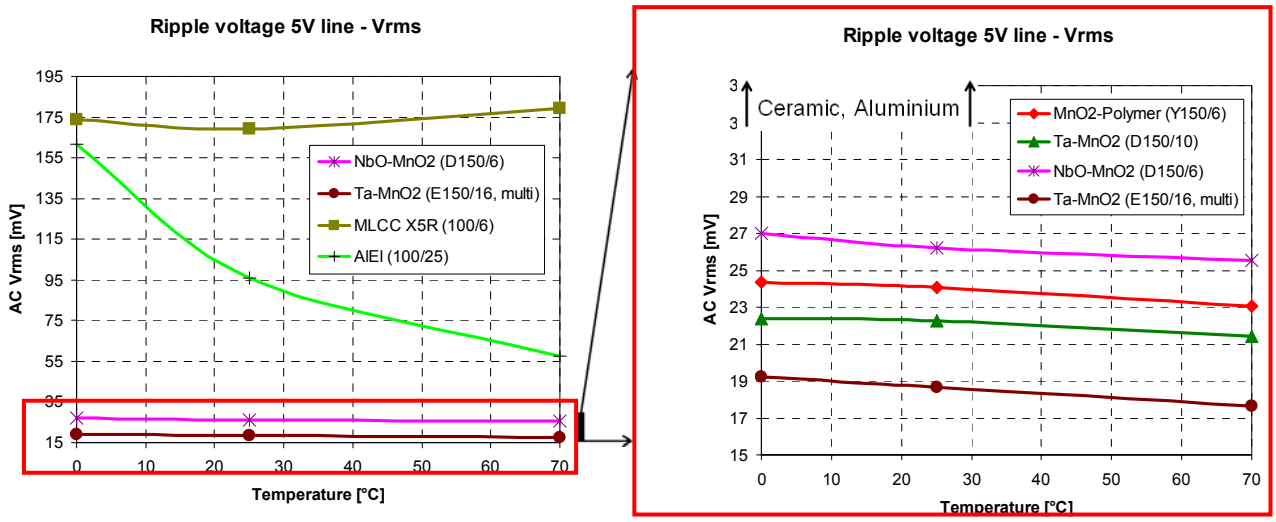


Figure 22 a: b:

5V output Vrms of ripple voltage benchmark, magnified scale on right side

Aluminium electrolytic and MLCC capacitor Vrms behaviour across a wide Vrms range is displayed in Figure 21a and Figure 22a . Figure 21b and Figure 22b show a much smaller range in magnified scale. For both outputs and most of the capacitor technologies the output ripple Vrms decreases with increasing temperature in a nearly linear fashion. Aluminium electrolytic and MLCC capacitors are exceptions due to the exponential change in capacitance and ESR they exhibit with temperature (see Figure 17 and Figure 18). Aluminium electrolytic capacitors also exhibit a too high level of ESR across the temperature range, so their smoothing ability is limited, as the output ripple voltage is much higher than with other technologies. When MLCC is used with the very low ESR levels circuit instabilities result, so output ripple voltage is also high. Among the other technologies we can observe that ripple voltage at the output will be lower when ESR is low and capacitance at switching frequency is high.

Summary

Table of output capacitor preliminary static measurements

Capacitor technology	Level of the ESR at f_{sw} = 300 kHz	Capacitance stability vs. temperature	Capacitance stability vs. DC voltage bias	ESR stability vs. temperature
Ta-Polymer	++	+	+	++
Ta-MnO_2 (single)	+	++	++	+
NbO-MnO_2	+	+	+	+
Ta-MnO_2 (multi)	++	++	++	+
MLCC	- (too low)	0	-	++
Aluminium El.	- (too high)	-	++	-

Explanation: ++ very good, + good, 0 neutral, - poor

Table showing output capacitor application measurements

Capacitor technology	AC Vrms at 25 °C	Vrms stability vs. temperature	Case size
Ta-Polymer	+	++	++
Ta-MnO_2 (single)	+	+	+
NbO-MnO_2	0	0	+
Ta-MnO_2 (multi)	++	++	0
MLCC	-	-	+
Aluminium El.	-	-	-

Explanation: ++ very good, + good, 0 neutral, - poor

- Low output ripple voltage for the DC/DC converter can be achieved using output capacitors with low ESR at the switching frequency - in our case Tantalum-polymer and Tantalum-MnO_2 multi-anode capacitors. The rate of decrease of the actual capacitance with frequency in relation to the resonance frequency is also important.
- Tantalum-MnO_2 capacitors are recommended in applications with variable output voltages because they offer the best capacitance stability versus DC bias voltage.
- It is strongly recommended that designers consider the capacitance and ESR temperature stability of output capacitors when deciding on the system's operating temperature. From this point of view, Tantalum-Polymer and Tantalum-MnO_2 capacitors were found to be the most stable, whereas MLCC and Aluminium-electrolytic capacitor are the least stable.
- Comparing capacitor size: in our benchmark, Tantalum-Polymer and Tantalum-MnO_2 low profile capacitors were the smallest suitable capacitors followed by Niobium Oxide-MnO_2 with the same footprint but a little higher in profile. Aluminium-electrolytic radial leaded capacitors require a bigger footprint and are much larger in volume.

Conclusions and Recommendations

- As the main energy carrier, the output capacitor plays an important role in DC/DC switching converter functionality. The capacitance and ESR of the output capacitor can significantly influence the DC/DC converter regulator feedback loop, which defines the stability of the converter operation. These parameters have to be in a certain range to assure stability of the system. In our experiments, MLCC output capacitors had too low an ESR (in range of 1 – 2mΩ), which resulted in oscillations of the circuit and a relatively high ripple voltage. Therefore, MLCC devices cannot be recommended based on the findings of our experimental study. The use of MLCC capacitors can be recommended only following a careful evaluation of their low ESR versus stability of the loop.
- Using of generic Aluminium electrolytic capacitors resulted in high output ripple voltage and poor filtering due to their higher ESR characteristics. This also significantly deteriorates at lower temperatures.
- Based on our measurements using the Maxim MAX1537EVKIT evaluation kit we can conclude that

using low ESR output capacitors such as Tantalum-Polymer and Tantalum-MnO_2, especially with a multi-anode construction, leads to the best results measured by AC Vrms of output ripple voltage and Vrms temperature stability. MLCC and Aluminium Electrolytic technologies can be used as long as attention is paid to the instability (MLCC) and output ripple (Aluminium). Good cost versus performance value can be also achieved using NbO capacitors.

References

1] Maxim MAX1537 main power supply controller datasheet and product flyer: http://www.maxim-ic.com/quick_view2.cfm/qv_pk/4521

2] C. Simpson, Member of Technical Staff, Power Supply Design Group, National Semiconductor

3] SMPS datasheets from Maxim, National Semiconductor, Linear Technology, ON Semiconductor, Texas Instruments and other SMPS manufacturers, available at:

http://www.maxim-ic.com/products/power/dc_dc_switchers/
http://www.national.com/analog/power/simple_switcher
http://www.linear.com/pc/viewCategory.jsp?navId=H0,C1,C1003,C1042
http://www.onsemi.com/PowerSolutions/parametrics.do?id=149
http://focus.ti.com/paramsearch/docs/parametricsearch.tsp?family=analog&familyId=490&uiTemplateId=NODE_STRY_PGE_T

4] Maxim MAX1537EVKIT evaluation kit datasheet and product flyer: http://www.maxim-ic.com/quick_view2.cfm/qv_pk/4546

5] HP Impedance analyser 4192A description and datasheet:
http://www.testequipmentdepot.com/usedequipment/hewlettpackard/impedanceanalyzers/4194a.htm

6] Agilent Infiniium oscilloscope 54830B datasheet:
http://www.datasheetcatalog.org/datasheet2/9/0o4ptsp0alkuqg2rh3tp0wy3expy.pdf

7] T. Zednicek, B. Vrana et al., *Tantalum and Niobium Technology Roadmap:*
http://www.avx.com/docs/techinfo/tantniob.pdf

8] T. Zednicek, *Tantalum Polymer and Niobium Oxide Capacitors*:
http://www.avx.com/docs/techinfo/newtant.pdf